14.2 All Digital Spread Spectrum Clock Generator for EMI Reduction

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Electromagnetic interference (EMI) in electronic products such as home theater systems or DVD players is a real issue that must be dealt with. Among all the techniques used to reduce the radiated power, a popular one is to modulate the system clock of the computing devices such that the radiated power level in a given bandwidth is lower. The standard bandwidth for this type of measurement is 120kHz. This technique is called spread spectrum clock generation (SSCG).

The commonly used technique to produce SSCG is an "all analog" one where modulation is applied or inserted into a phased lock loop (PLL). The frequency can be modulated by imposing a signal on the voltage control node of a VCO [1] or by using a "fractional N" technique that changes the divider ratio [2]. The technique presented in this paper does not use any PLL or "analog" circuits. The circuit (0.06mm^2) is fabricated in a 0.15µm CMOS process and consumes 7.1mW for the application of 27MHz.

The entire circuit is based on a digital delay line (DDLi) with a small logical circuit to control it. The DDLi is used to modulate an input clock. The size of the DDLi is limited to one period of the input clock and several techniques are developed to allow adequate frequency modulation and frequency deviation. The principle logic circuits used include the "wrap around circuit" (the removal of one period delay in the delay line), the circuit that cancels one intrinsic delay inside the DDLi and the circuit that performs calibration.

The DDLi is made from 384 (24×16) inverter buffers placed on a matrix multiplexer. The first 16 taps are duplicated and each of their outputs is connected to a bank of D-type flip-flop as shown in Fig. 14.2.1. This arrangement is used to monitor the arrival of the rising edge in the DDLi. In the design of the duplicated row, it is critical to compensate the delay of the multiplexer switch with the same delay in front of the duplicated row. The remaining uncompensated delay is the delay from the output of the clock to the input clock of the D-type flip-flop and this delay is cancelled out in the digital section. Figure 14.2.2 shows the basic delay cell and Fig. 14.2.3 shows the actual delay of approximately 200ps. The delay cell is made with two NMOS devices driven with a differential signal from the previous cell. The NMOS load is a pair of cross-coupled PMOS devices inside the box labeled "pload" (see Fig. 14.2.2). It is basically a differential input / differential output inverter. Each delay cell drives the following identical cell. The wire X and Z in that cell are the grid of the matrix multiplexer. The delay cell is connected to the lower gates all the time so that the delay does not change when the row is selected. So each delay cell sees the same load.

The logical circuit designed to control the DDLi is shown in Fig. 14.2.4. For a desired frequency modulation and frequency deviation, the user sets registers in the calibration module. This calibration is done by searching for the number of taps per period and hence takes into account the variable delay per tap automatically. This delay per tap can vary with temperature and process and since the circuit measures this variable continuously, the circuit remains calibrated. Based on the request and the number of taps per period calculated by the same module, a triangular wave is set to the required frequency and amplitude. By integrating this wave, we obtain the required delay on the DDLi to produce the modulated clock with a down spread. A decoder is required to control the DDLi. When the actual delay of the delay line becomes one period in length the Q output of the flip-flop in the DDLi will show the exact location of the rising edge (the future rising edge) and then the wrap around module will reset the integrator to remove one period of the clock exactly. This process of removing one period of the clock in the DDLi can be done to within one tap delay of accuracy by using the position of the edge as sampled by the bank of flip-flops. However, the delay between the output (or modulated) clock and the input clock of the flip-flop creates a discontinuity in the wrap around. This delay is compensated for in the digital section with an adaptive circuit. The adaptive circuit can monitor the successive rising edges in the bank of flip-flops and so can detect the discontinuity when the wrap around is applied. This discontinuity is then removed by successively reducing the error in a simple control loop.

The functional description of the circuit in the previous paragraph was for a down spread modulation. In the case of an up spread modulation, one would think that a set of flip-flops at the end of the DDLi would be required. Such an additional monitoring device is not required, since the logic circuit keeps track of the number of taps per period and hence can wrap around in the other direction as well without a glitch. The same correction to the intrinsic delay can still be performed the same way. As a result, the circuit can perform up or down spread without limitations.

There are many ways to look at the performance of the SSCG. Figure 14.2.5 shows the simulation of the circuit when up and down spread is set. The plot shows for each successive clock cycle the corresponding period of the clock. For this simulation, an ideal delay line is used with a fixed delay of 200ps for each tap. Figure 14.2.6 is the spectrum of the clock as measured from the chip. The resolution bandwidth and the video bandwidth for this measurement is 100kHz. The reduction of peak power from the reference clock is 13dB for a deviation of about 6% and a frequency modulation of 100kHz. A peak power reduction of more than 7dB is measured for a deviation of 1.6%.

As it can be seen in Fig. 14.2.6, the measured frequency of the SSCG is the output of a PLL operating at 121.5MHz, 4.5 times the reference. One advantage of this circuit is that no modification to the 27MHz reference or the system PLL was required in order to generate the spread spectrum clock.

An "all digital" spread spectrum clock generator is presented. The circuit can perform up and down spread relative to the nominal frequency with programmable and calibrated frequency deviation and frequency modulation. A peak power reduction of 13dB was measured.

References:

[1] Hsiang-Hui Chang, I-Hui Hua and Shen-Iuan Liu, "A Spread-Spectrum Clock Generator With Triangular Modulation," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 673-677, April, 2003.

[2] Wei-Ta Chen; Jen-Chien Hsu; Lune, H.-W.; Chau-chin Su, "A Spread Spectrum Clock Generator for SATA-II," *IEEE International Symposium on Circuits and Systems*, pp. 2643-2646, May, 2005.

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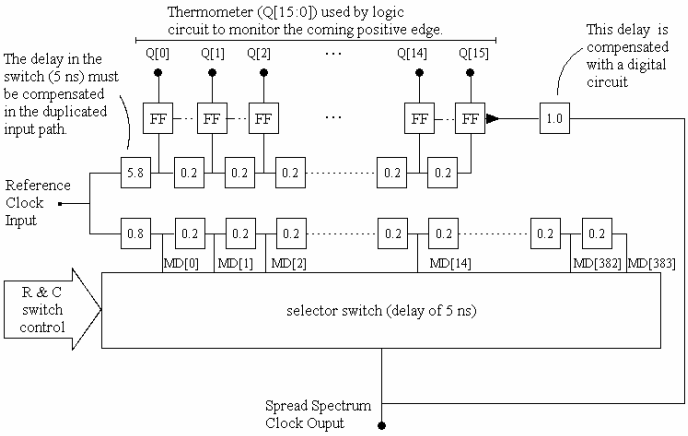


Figure 14.2.1: Block diagram of the digital delay line.

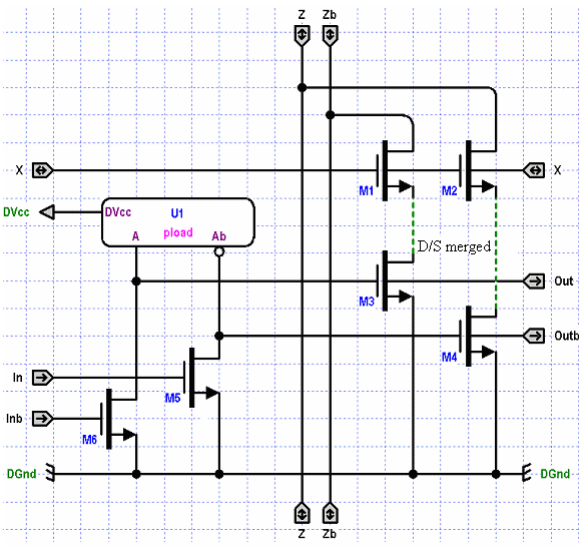


Figure 14.2.2: Schematic of a single cell in the digital delay line.

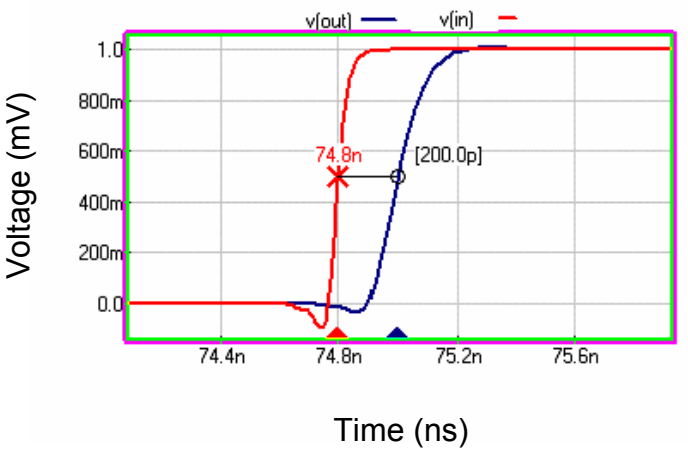


Figure 14.2.3: Time delay of a single cell in the digital delay line.

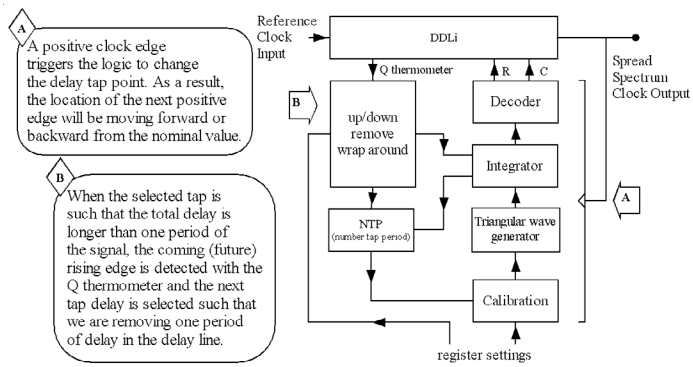


Figure 14.2.4: Block diagram of the entire SSCG circuit.

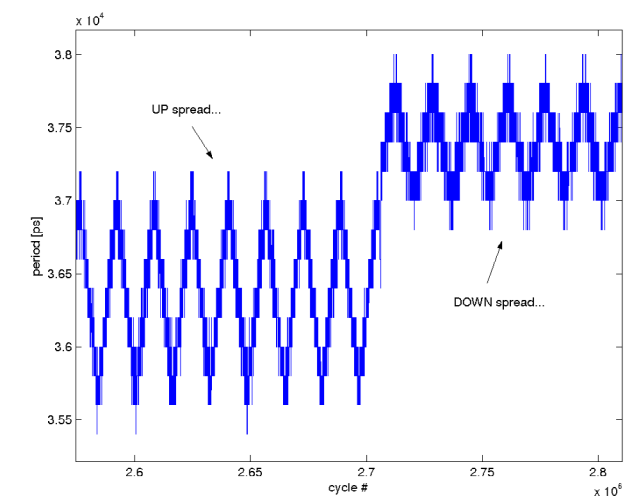


Figure 14.2.5: Simulation of the circuit showing the period of each cycle for a up spread and a down spread configuration.

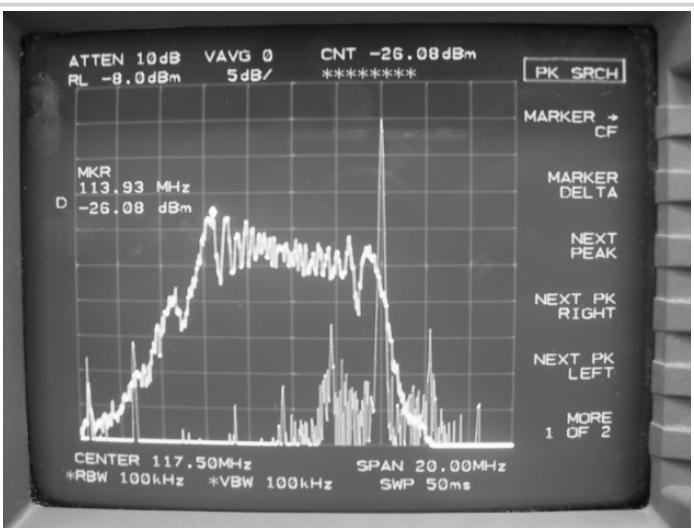
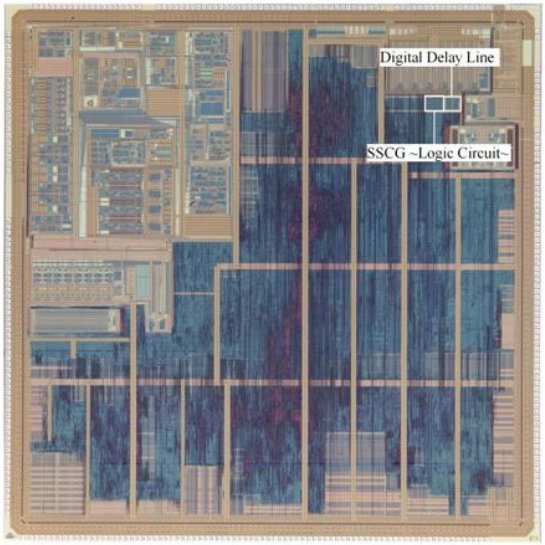


Figure 14.2.6: Measured spectrum of the SSCG clock with 6% frequency deviation and 100kHz frequency modulation. A 13dB peak power reduction is observed.

Continued on Page 652



14.2.7: Chip micrograph. Total area for the SSCG circuit is 0.06mm^2.

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